What is claimed:

1. A non-volatile semiconductor memory device comprising:

a semiconductor substrate;

an impurity region and an element isolation region formed in the semiconductor substrate; and

first and second memory elements mutually isolated by the element isolation region,

the impurity region including a first impurity diffusion layer and a second impurity diffusion layer,

the first memory element and the second memory element each including a gate dielectric layer, a floating gate, a selective oxide dielectric layer and a third impurity diffusion layer, also including a common intermediate dielectric layer and a common control gate, and being connected to the first and second impurity diffusion layers,

the third impurity diffusion layer located in each of the first and second memory elements including a channel region, and

an impurity concentration of the third impurity diffusion layer located in the first memory element being different from an impurity concentration of the third impurity diffusion layer located in the second memory element.

2. A non-volatile semiconductor memory device according to claim 1, wherein the first impurity diffusion layer is electrically connected to a bit line.

3. A non-volatile semiconductor memory device according to claim 1, wherein a threshold voltage of the first memory element and a threshold voltage of the second memory element are set at different values.

4. A non-volatile semiconductor memory device comprising:

a semiconductor substrate;

an impurity region and an element isolation region formed in the semiconductor substrate; and

first and second memory elements mutually isolated by the element isolation region,

the impurity region including a first impurity diffusion layer and a second impurity diffusion layer,

the first memory element and the second memory element each including a gate dielectric layer, a floating gate, a selective oxide dielectric layer and a third impurity diffusion layer, also including a common intermediate dielectric layer and a common control gate, and being connected to the first and second impurity diffusion layers,

the first impurity diffusion layer being electrically connected to a bit line,

the third impurity diffusion layer in each of the first and second memory elements including a channel region, and

a threshold voltage of the first memory element and a threshold voltage of the second memory element being set at different values.

5. A non-volatile semiconductor memory device according to claim 4, wherein the first memory element and the second memory element are electrically connected to a common bit line through the first impurity diffusion layer.

6. A non-volatile semiconductor memory device according to claim 5, further comprising an interlayer dielectric layer formed over the first memory element and the second memory element and a contact section passing through the interlayer dielectric layer,

wherein the first impurity diffusion layer is connected to the bit line through the contact section.

7. A non-volatile semiconductor memory device according to claim 4, wherein the third impurity diffusion layer included in each of the first and second memory elements is formed in a section between the first impurity diffusion layer and the second impurity diffusion layer, and immediately below the gate dielectric layer and the control gate.

8. A non-volatile semiconductor memory device according to claim 4, wherein three types of data can be written and read.